



Choosing a high-speed logic analyzer probe

*The test engineer must be aware of the factors involved
in today's specialized signal integrity testing*

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Over the past decades, digital designers have relied on the logic analyzer as their main tool for system validation. In recent years, faster clock rates have forced designers to consider signal integrity in all parts of their systems, including testability.

No longer can logic analyzer probes be arbitrarily connected to the system with ensured success. Considerations such as probe location, loading, and vicinity to the transmission line must be examined.

The goal of any type of probe is to present the smallest electrical load to the system as possible. If the probe alters the performance of the system too drastically, the probe does not help the designer validate a system because the cause of failure may be entirely due to the probe.

The isolation of the failure is important to effective validation of a failure. Thus, the designer must be able to predict the effect of the probe on the system whether it is negligible or dominant.

Predicted performance

The most accurate way to predict the performance of a probed system is to include a probe load model in the system simulations. Logic analyzer vendors provide RLC circuits that model their probe loads up to a predefined frequency (usually 6 GHz).

Simulations not only provide the most accurate model of the probe's effect, they also provide a way to alter variables and monitor each variable's effect. These variables include probe location on the transmission line, and/or probe stub length from the transmission line to the probe tip. In general, a logic analyzer probe will appear as in *Fig. 1*.

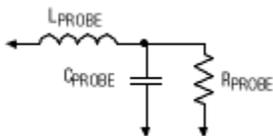


Fig. 1. A logic analyzer probe can be characterized as an RLC network.

At lower frequencies, the resistor will dominate the probe's impedance and will have minimal effect on the target because the probe impedance is on the order of 20 k Ω and the target typically appears as 50 to 75 Ω . The two impedances are in parallel and yield most nearly the target impedance. As the frequency goes up, the probe will begin to look capacitive and its impedance will start to roll off.



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Once the impedance approaches the order of magnitude of the target, reflections from the probe become an important issue. At very high frequencies, the probe looks inductive and the impedance will increase.

Resonance

The capacitive and inductive nature of the probe load forms a resonance. The goal of the logic analyzer probe is to push its resonance as far up in frequency as possible.

In addition, the impedance at resonance should be as high as possible. If the probe impedance gets within the range of 10 to 20 Ω , the probe will shunt out the higher frequency components of the target system.



For each probing form factor, the vendor will provide exact load models and the impedance vs. frequency profile. For a quick estimate of the probe's effect, logic analyzer probe vendors provide a lumped-capacitance estimate of each probing form factor. With the equivalent lumped capacitance, a time constant is formed with either the termination resistance or the impedance of the transmission line.

This equivalent capacitance can then be used in an rms sum of the time constants in the system. Once the overall system time constant is found, this can be converted to rise time and bandwidth to predict the contribution of the probe to the overall performance of the system.

Probing location

Since the probe is part of the circuit and the circuit is part of the probe, the effect at both points of interest--receiver and probe tip--can be predicted. One of the probe's largest influences is the impact of its location on the target transmission line.

The reflections that the probe causes will be determined by its relative position on the transmission line. Whether or not the reflections are of severe impact depends on the target system--trace length, termination scheme, voltage margin, and so forth. *Figure 2* shows a standard transmission line system highlighting the most common locations where a logic analyzer probe can be connected.

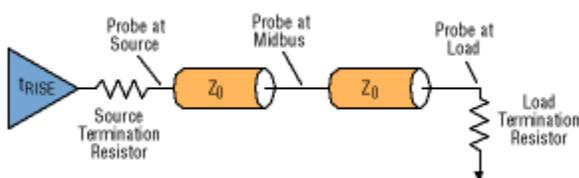


Fig. 2. The point at which the probe contacts the transmission line affects the readings obtained.

Load-terminated system

In a load-terminated system, only the load termination resistor is used in the transmission line design. Reflections that are induced are absorbed into the termination resistor at the receiver.

If these reflections arrive at the same time as the incident wave or subsequent waves, they manifest themselves as rise-time degradation or intersymbol interference (ISI).

When connecting a logic analyzer probe to the system, the probe will look like a capacitive discontinuity. The best location to insert the probe in this type of system is at the source.

The first reason for this is that the reflection off of the probe occurs instantaneously at the driver. This reflection then re-reflects off of the low impedance driver and travels down the transmission line with the incident wave.

The received waveform experiences rise-time degradation but has minimal secondary reflections. Second, to reduce the effect of the capacitive load on the system, the RC time constant formed by the probe should be as low as possible.

The capacitance of the probe cannot be changed, but the resistance/impedance of the time constant will depend on the location of the probe. By inserting the probe at the source, the resistance/impedance of the time constant is the parallel combination of the low impedance driver with the transmission line impedance. This combination yields the lowest resistance/impedance in the system and hence the lowest RC time constant.

Source-terminated system

In a source-terminated system, only the source termination is used. The incident wave divides in amplitude across the source termination resistance and the impedance of the transmission line.

The half amplitude wave travels to the receiver where it experiences a 100% positive reflection. This reflection superimposes itself with the incident wave to yield the original amplitude of the driver.

The reverse traveling reflection propagates back to the driver where it is absorbed into the source termination resistor. The architecture of a source-termination is such that at any place on the transmission line besides exactly at the receiver, the waveform observed will have a stair-step shape.

A logic analyzer decides whether the signal being probed is a 1 or a 0 by comparing it with a user-defined threshold voltage (typically centered in the voltage swing). This means that if the logic analyzer probe is located anywhere besides directly at the receiver, it will observe this stair-step waveform shape.

For the duration of time that the waveform resides in the middle of the swing, the logic analyzer will not be able to determine the logic level. This directly affects the timing performance of the analyzer and the logic analyzer probe should be placed as close to the receiver as possible.

Double-terminated system

In a double terminated system, both the source and termination resistor are used in the transmission line. In this system only half of the original signal will reach the receiver because of the resistive divider formed by the source and load termination resistor.

The logic analyzer probe can typically be placed anywhere on this type of system. The main consideration is the RC time constant of the probe.

However, at any location on the system, the resistance/impedance will be half of the characteristic impedance of the line. Since only half of the original voltage level will be observed at the probe tip, the engineer must make sure that the logic analyzer *minimum voltage swing* specification is met.

Stub probing

When the probe tip cannot be placed directly on the target's transmission line, the length of trace that runs between the probe tip and the target signal is called a stub. The stub can consist of a pc-board trace, wire, or the leads of a connector.

Stub probing is difficult to avoid due to layout constraints on a pc board. The question then becomes how close does the probe tip need to be to the transmission line to give acceptable performance in the system and in the logic analyzer?

For a logic analyzer, the recommendation is that the stub has an electrical length of no more than 20% of the system rise time. For an electrical length that is less than 20% of the system rise time, the stub can be treated as a lumped capacitance and not a distributed transmission line.

However, the capacitance increases greatly as the stub length increases. At a point, the trace capacitance will exceed the total capacitance of the probe.

Damped-resistor probing

Clearly the addition of a transmission line stub between the probe tip and the probed system can severely affect the signal quality at both the receiver of the target and at the probe tip of the logic analyzer. One way to improve the performance of the probe and system when the probe tip cannot be placed directly on the target system is a method called damped-resistor probing.

By inserting a damping resistor directly at the target, a longer stretch of stub can be tolerated to the probe tip. The damped resistor serves two purposes--it isolates the target system from the capacitive loading of the stub probe, and it dissipates the energy of the reflections on the stub so that the logic analyzer observes a cleaner signal.

Technique

Probing techniques are even more important in modern logic analyzers that contain signal integrity tools such as "Eye Scan" by Agilent Technologies. Logic analyzers are providing analog insight into the behavior of the signals being probed.

In order for this analog information to be of any use, the probe itself must not distort the waveform being displayed. If the probe loading can be minimized, then the eye diagrams that are produced can be accepted as a true analog representation of what is happening in the system.

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