

## Brock J. LaMer

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### A. Professional Preparation

Montana State University, Bozeman, MT	Electrical Engineering	B.S., 1998
University of Colorado, Colorado Springs, CO	Electrical Engineering	M.S., 2001
University of Colorado, Boulder, CO	Electrical Engineering	Ph.D., 2005

### B. Appointments

Assistant Professor 7/06-present	Montana State University Electrical & Computer Engineering Bozeman, MT 59717
R&D HW Engineer 1/99–7/06	Agilent Technologies Digital Validation Division Colorado Springs, CO 80907
Research Assistant 5/97-12/98	Montana State University Electrical & Computer Engineering Bozeman, MT 59717

### C. Publications (over 40 total)

"Off-Chip Coaxial to Microstrip Transition Using MEMs Trench" LaMer & McIntosh, 13<sup>th</sup> NASA Symposium on VLSI Design, June 2007.

"Bus Stuttering: An Encoding Technique to Reduce Inductive Noise in Off-Chip Data Transmission", LaMer and Khatri, Design Automation and Test in Europe, March 2006.

"Impedance Matching Techniques for VLSI Packaging", Brock LaMer, Kanupriya Gulati, Rajesh Garg, & Sunil Khatri, DesignCon 2006, February 2006.

"Controlling Inductive Cross-talk and Power in Off-chip Buses using CODECs", LaMer, Gulati, and Khatri, Asia and South Pacific Design Automation Conference (ASP-DAC), 2006.

"Broadband Impedance Matching for Inductive Interconnect in VLSI Packages", B.J. LaMer and S.P. Khatri, IEEE International Conference on Computer Design (ICCD-2005), October 2, 2005. [Best Paper Award : Circuit Consideration in Process Design](#)

"Performance Model for Inter-chip Communication Considering Inductive Cross-talk and Cost", LaMer and Khatri, IEEE Symposium on Circuits and Systems (ISCAS-05), May 23, 2005.

"Encoding-based Minimization of Inductive Cross-talk for Off-chip Data Transmission", B.J. LaMeres and S.P. Khatri, Design Automation and Test in Europe (DATE-05), March 13, 2005.

"Performance Model for Inter-Chip Busses Considering Bandwidth and Cost", B.J. LaMeres and S.P. Khatri, DesignCon 2005, February 2, 2005.

[Best Paper Award : Board Level Design Track](#)

#### D. Synergistic Activities

Invited Talk: "Challenges in Debugging at 5GHz",  
Brock LaMeres, John Calvin, & Sarah Boen  
Intel's Developers Forum (IDF-Fall-05), San Francisco, CA. August 23, 2005.

Invited Talk: "Compensation for Simultaneous Switching Noise in VLSI Packaging",  
Brock LaMeres,  
MCEN 5166 - Electronic Packaging Class, University of Colorado, Boulder. September 15, 2005.

Patent: "Incorporation of isolation resistor(s) into probes using probe tip spring pins",  
Brock J. LaMeres, Brent A. Holcombe & Glenn Wood. US Patent 7,183,781, February 27, 2007.

Patent: "Apparatus, method, and kit for probing a pattern of points on a printed circuit board",  
Brock J. LaMeres, Brent A. Holcombe & Kenneth Johnson. US Patent 7,145,352, December 5, 2006.

Profession Membership: IEEE, Member, (1998-present), Registered Professional Engineer, Colorado, Registration # 37255, (12/30/02 - present), Registered Professional Engineer, Montana, Registration # 13627, (11/8/06 - present), Technical Program Committee, DesignCon (5/03 – present), Editor, "Active and Passive Electronic Component Journal – APEC (9/06 – present).

#### E. Collaborates & Other Affiliations

(i) *Collaborators:* Dr. Richard Wolff, Montana State University - Bozeman  
Dr. Hashem Nehrir, Montana State University - Bozeman  
Dr. Todd Kaiser, Montana State University - Bozeman

(ii) *Graduate Advisors:* Dr. T.S. Kalkur, University of Colorado – Colorado Springs Dr.  
Dr. Sunil P. Khatri, Texas A&M University – College Station

(iii) *Student Advising:* Chris McIntosh, Montana State University - Bozeman  
Srinitha Nimmakayala, Montana State University – Bozeman  
Charles Ostrander, Montana State University – Bozeman