

## EE317 Electronics

**Fall 2009**

**4 credits**

**Course Webpage:** <http://www.coe.montana.edu/ee/davidd/ee317/ee317.html>

**Course Listserv:** [ee31701@listserv.montana.edu](mailto:ee31701@listserv.montana.edu)

**Class meetings:** MWF 9:00-9:50 Roberts 218 *lecture*  
T 12:00-2:00 Cobl 621 *lab section 1*  
T 2:10-4:00 Cobl 621 *lab section 2*  
T 4:10-6:00 Cobl 621 *lab section 2*

**Instructor:** David Dickensheets  
530 Cobleigh Hall  
994-7874  
[davidd@ee.montana.edu](mailto:davidd@ee.montana.edu)  
Office Hours: TBA

**Teaching Assistant:** Ningkonsin Rajkumar, 528 Cobleigh

**Grader:** Adel Nehmeh, 638 Cobleigh

**Text:** *Microelectronic Circuits*, 5<sup>th</sup> Edition, by Sedra and Smith (Oxford, 2004).

**Other Resources:** *The Art of Electronics*, 2<sup>nd</sup> Edition, Horowitz and Hill (Cambridge, 1989).

**Prerequisites:** EE207

### **Course Description:**

ELECTRONICS: A branch of electrical engineering; the science and technology based on and concerned with the controlled flow of electrons (or holes).

This is an introductory course in electronics. It introduces diodes, bipolar junction transistors, field effect transistors and bipolar and MOS analog and digital circuits.

### **Course Organization and Grading:**

There will be three lecture periods each week, and one two-hour lab. There will be homework assignments, and you will turn in four formal lab reports.

Homework and quizzes	15%
First Midterm Exam	20%
Second Midterm Exam	20%
Final Exam	20%

(The final exam is scheduled for  
Thursday, Dec. 17 from 8:00 – 9:50am)

Laboratory Grade 25%

The laboratory grade will be composed of several parts as follows:

Attendance ≤ 2 unexcused absences for passing grade

Notebooks 25%

Prelabs 15%

Formal reports 60%

**Passing the laboratory portion of the course requires a score of at least 50% for the laboratory grade. You must pass the laboratory portion of the class to pass EE317.**

You will keep a laboratory notebook documenting all of your experiments and calculations in the lab. This notebook should be bound, with numbered pages. Notebooks will be handed in for grading on the following dates:

September 16 (after the second lab period)

December 7

The notebook grade will be awarded based on completeness of recorded data, including diagrams of circuits, complete description of signal sources and measurement techniques, tabular data and graphical data, along with enough narrative to describe the experiments. Neatness counts.

Prelabs are to be completed *in your notebooks*, preceding the day's experimental data. You must have the lab instructor initialize the prelab at the beginning of the lab period. Prelabs without the instructor's initials will receive zero credit. Prelabs will be graded at the same time that notebooks are graded.

You will be required to hand in four formal lab reports. These will be due according to the following schedule:

First report on or before September 28

Second report on or before October 19

Third report on or before November 23

Fourth report on or before December 7

The format for formal lab reports will be provided in a separate document.

## Course Policies

Late work will not be accepted.

Do your own work.

Working together to solve homework problems is encouraged. You should learn from one another! However, the work you hand in should be your own. The “committee” approach to homework of divvying up the problems amongst your group and copying the solutions from your friends is cheating and will not be tolerated. You learn by doing, so please do your own work.

There will be guidelines handed out separately for the lab sections.

## What you should expect from this class

After completing this class, you should be familiar with the following topics:

- operational amplifier device properties
- operational amplifier circuits
- $pn$  junction diode forward and reverse I-V characteristics
- zener diodes and applications
- spice modeling of  $pn$  junction diodes
- field effect transistor (FET)
- FET dc biasing
- FET modeled as a two-port device
- FET ac analysis
- spice modeling of FET circuits
- integrated circuit MOSFET circuit design concepts
- bipolar junction transistor (bjt)
- bjt dc biasing
- bjt modeled as a two-port device
- bjt ac analysis
- common emitter, common base and common collector configurations
- spice modeling of bjt circuits
- output stage amplifiers
- CMOS and TTL logic building blocks
- CMOS and TTL properties