

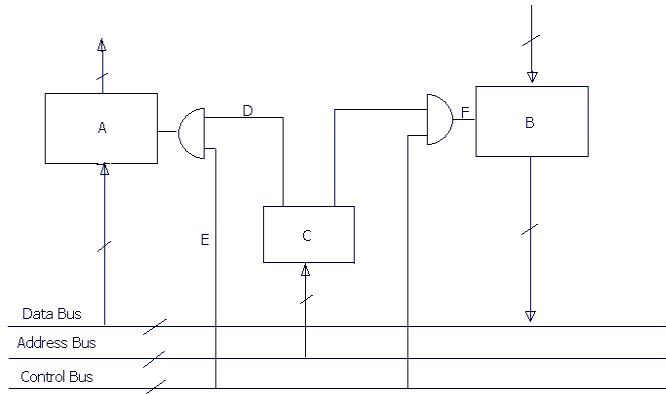
Please put your name on the outside of the paper also.

Name _____ Key _____

OPEN BOOKS, OPEN NOTES.

Hand in the test folded so your name shows on the outside.

An I/O interface is shown in the diagram below. Answer question 1 based on this diagram. (18 points)



1. Give the name and a description of the function of each of the labeled elements:

	Name	Function
Element A	Output Latch_____	Latch data from DB to hold for external output device_
Element B	Input tristate buffer____	Get input data onto DB at the correct time_____
Element C	Address Decoder_____	Decode correct input and output device addresses_____
Signal D	ADR_OK_____	Asserted when output address is OK_____
Signal E	Write Control_____	Asserted when CPU has put data on the data bus_____
Signal F	Tristate enable_____	Asserted when CPU ready to take data and address is OK

2. Briefly describe how a processor determines the address of the interrupt service routine for each of the following types of interrupting systems: (6 points)

a. Polled:

When an IRQ occurs, S/W interrogates (polls) each device until it finds which one did it and then branches to the correct ISR.

b. Vectored:

Hardware sets the interrupt request and each device has a specific memory location which contains the starting address of the ISR for that interrupt.

3. List three ways to synchronize I/O software. (3 points)

- Software delays_____
- Polling or handshaking_____
- Interrupts_____

4. “An interrupt system must allow asynchronous events to interrupt an ongoing process.”

Give five more attributes of an interrupt system. (5 points)

- Must get to correct ISR_____ Must finish current instruction_____
- Must handle simultaneous interrupts_____ Must handle sequential interrupts_____
- Must have global program control_____ Must have individual program control_____
- Must preserve the machine context_____ Must allow a variety of interrupting signals_____
- Must return to interrupting program_____

An intelligent 68FC12 processor has the following pinouts:

<u>Signal</u>	<u>Function</u>	<u>Direction</u>
ADR11-ADR0	12 address bits	output
DB7-DB0	8 data bits	bidirectional
RD	Read control	output, active high
WR	Write control	output, active high
INTR	Interrupt request	input, active high

Answer the following questions 5 - 7 based on this information: (3 points)

5. Are the I/O addresses in this processor memory mapped or is there a separate I/O address space?
Memory Mapped
6. What is the total address space available?
 $2^{12} = 4096$ bytes
7. In this processor, how many bits must be decoded to fully decode an I/O address.
12 bits

For the multiple choice questions below, choose the most correct answer (10 points.)

8. A tristate driver is used to allow
 - a. multiple destinations to exist on a data bus
 - b. multiple sources to exist on a data bus with only one active at a time
 - c. multiple sources to exist on a data bus with more than one being active at a time
 - d. a source to write into more than one destination at a time
 - e. none of the above.
9. In the HC12, Port H is
 - a. input only
 - b. output only
 - c. bidirectional
 - d. none of these
10. For a processor with 10 interrupting devices, which type of architecture provides the fastest transfer of control to the interrupt service routine for a specific interrupt?
 - a. Polled
 - b. Vectored
 - c. Both offer the same performance
11. Which type of I/O addressing uses memory reference instructions to access I/O devices?
 - a. Separate I/O
 - b. Memory mapped I/O
 - c. Neither
 - d. Both
12. Which type of I/O addressing requires more expensive address decoders?
 - a. Separate I/O
 - b. Memory mapped I/O
 - c. Neither
 - d. Both