

EE 371 Second Semester Test - Tuesday October 29, 2002  
35 Points, 16.667% of Final Grade

Please put your name on the outside of the paper also.  
Hand in the test folded so your name shows on the outside.

Name \_\_\_\_\_KEY\_\_\_\_\_

1. A 371 student has written the following module to complement a data byte. (4 points)

```
1 ; Subroutine
2 compl_byte:
0000 B66000 3 ldaa data_byte
0003 41 4 coma
0004 7A6000 5 staa data_byte
0007 3D 6 rts
```

- a. In addition to not having sufficient comments, it doesn't conform to the coding standards published for EE371. What is wrong?

**Registers are modified in the subroutine**

- b. What would you do to fix the code (don't worry about the comments).

**Add psha at the beginning and pula at the end.**

2. The data in memory locations \$6000 - \$600F, as shown by an MD 6000 command is:

6000 60 03 88 60 - 05 83 60 06 - 20 48 65 6C - 70 4D 65 21 `.`.... HelpMe!

Give the results (in hex) of the following instructions which are executed in sequence. (5 points)

```
ldx #6000 X = $6000
ldaa 4,X A = $05
ldab A,X B = $83
ldy 3,X Y = $6005
cmpa 0,y
bgt someplace Branch taken? Yes
```

3. Write a structured assembly language code segment for the following pseudo code design:  
 Assume P, Q and R are 8-bit SIGNED integer variables in memory locations P and Q. Also assume function X is implemented in a subroutine named X.  
 Insert the code needed for the design in the comments below. You may add more comments if you wish.  
 (16 points)

```

; IF P does not equal Q
    ldaa P
    cmpa Q
    beq  endif
; THEN
;   P=R
    ldaa R    or    movb R,P
    staa P
; ENDIF P does not equal Q
endif:
; WHILE P < R
while_start:
    ldaa P    ; not really needed
    cmpa R
    bge  end_while
; DO P = P + 1
    inc  P
    bra  while_start
; ENDWHILEDO
end_while:

```

4. Give short answers to the following: (10 points)

a. What is a data bus?

**A parallel, bidirectional, binary information pathway with multiple sources and destinations.**

b. Why is an address decoder used in I/O interfaces?

**To select one-of-many sources or destinations.**

c. How is an information source, such as a set of switches interfaced to a data bus?

**With the use of tristate gates whose enable is controlled by an address\_OK signal and a READ control signal.**

d. What control signals are needed to latch data from the data bus into an output interface at the correct time?

**Address\_OK and WRITE**

e. Give the sequence of events that occur when a CPU does an input (or read) cycle.

**CPU puts address on the address bus**

**Address decoder generates ADR\_OK**

**CPU asserts READ control signal**

**Input device puts data on the data bus**

**CPU reads the data**

**CPU de-asserts READ control signal**