

EE 371 Third Semester Test - Thursday November 15, 2001
25 Points, 16.667% of Final Grade

Please put your name on the outside of the paper also. Name _____ KEY _____

Hand in the test folded so your name shows on the outside.

NOTATION NOTE: The notation /READ indicates an active-low (asserted-low) signal (READ_BAR).

1. Draw a timing diagram for a read cycle in a system that has a 16-bit address bus, 8-bit data bus and asserts /READ and /WRITE control signals. (8 points)
See Figure 7-8b on page 99 in M&M
2. For a CPU performing a write cycle, why does the CPU place the data on the data bus before asserting the /WRITE control signal? (2 points)
To satisfy the data setup time requirement of the latch.
3. Why must a tri-state gate be used to interface an input device to the data bus? (2 points)
To allow multiple sources to be used on the data bus.
4. Why must a latch be used to interface an output device to the data bus? (2 points)
The data bus is constantly changing with data flowing to and from memory and other I/O devices. The latch must be used to capture and hold the data for the output device. The latch must be clocked at the proper time.
5. Show how to wire up a single-pole, single-throw (SPST) switch to provide a logic signal. (2 points)
See Figure 7-22a, page 119, M&M
6. In the HC12, port H is a bidirectional port. Write a short segment of code that illustrates how to initialize port H so that bits 7, 6, and 5 may be used as outputs and 4, 3, 2, 1, and 0 may be used as inputs. (3 points)
DDRH EQU \$25
...
bset DDRH,%11100000 ; Make bits 7-5 output
bclr DDRH,%00011111 ; Make bits 4-0 input (optional)
7. In the HC12, how can a programmer control whether or not a higher priority interrupt request can interrupt the servicing of a lower priority interrupt? (2 points)
By selectively disabling lower priority interrupts and then unmasking global interrupts with the CLI instruction in the interrupt service routine.
8. In the HC12, why does the CPU automatically push all registers on the stack before transferring control to the user's ISR? (2 points)
To preserve the machine state or context.

What are the consequences of this CPU design decision? (2 points)

Increased interrupt latency compared to a design where the programmer is responsible for saving only the context that might be changed in the ISR.