

EE371 Third Semester Test – Thursday November 17, 2005  
40 points, 16.67% of Final Grade

Please put your name on the outside of the paper also. Name \_\_\_\_\_KEY\_\_\_\_\_

Notation: An active-low signal is denoted by an ‘\*’, i.e. ADR\_OK\* is a signal asserted low.

1. Assume K1 and K2 are signed, 8-bit integers and K3 is an unsigned, 8-bit integer number.
- a. Show how to allocate storage locations for these data variables (3 points)

K1 DS.B 1  
K2: DS.B 1  
K3: DS.B 1

- b. Write a structured assembly language code segment for the following portion of the design: (10 points)

```
; WHILE K2 < K1  
while_start:  
    ldaa   K2  
    cmpa   K1  
    bge    endwhile  
; DO  
; K1 = K1 - 1  
    dec    K1  
K2 = K2 + 1  
    inc    K2  
K3 = K3 + 1  
    inc    K3  
; ENDO  
    bra    while_start  
;ENDWHILEDO  
endwhile:
```

- c. Assume some other part of the program has initialized K1, K2 and K3 to the following values:

K1 = 3  
K2 = -4  
K3 = 0

What is the final value (in decimal or hex) expected for K1, K2 and K3 for this code?  
(3 points)

K1 = -1

K2 = 0

K3 = 4

2. Design an input interface to connect a set of 8 switches to a computer system using memory mapped I/O with an 8-bit data bus, 16-bit address bus and which produces a RD\* signal asserted when reading and WR\* signal asserted when writing. The interface is to input the data on the switches when an input operation is performed from address \$0100 and full address decoding is required. (6 points)

See Figure 7-9 in M&M

3. The infamous 68FC12<sup>1</sup> has a timer/counter similar to the HCS12 processor except its free running TCNT register is 10 bits and it is clocked by a 1 MHz clock. It has a timer overflow bit TOF, and one output compare register OC, with a OCF flag set when the comparison is made. It also has a separate input capture register IC and the ICF flag is set when a positive edge is seen on Port T bit 0. Each of these work just like the HCS12 output compare and input capture.(8 points)

- a. What is the interval between timer overflows?

$$1024 \text{ counts} * 1 \mu\text{s/count} = 1.024 \text{ ms}$$

- b. A program is needed using the output compare and interrupts to generate a 2 kHz waveform. What count should be added to the TC register each time an output comparison is made?

$$\text{The period is } 5 \times 10^{-4} \text{ sec, need OC every } 2.5 \times 10^{-4} \text{ sec} \times 10^6 \text{ counts/sec} = 250$$

- c. A routine to measure the frequency of a square wave using the input capture captures the TCNT register on rising edges. The first rising edge captures TCNT = \$010 and the second captures TCNT = \$100. What is the frequency of the square wave?

$$\text{\$100} - \text{\$010} = \text{\$0F0 counts} = 240 \text{ counts} \times 10^{-6} \text{ sec/count} = 2.4 \times 10^{-4} \text{ sec/period} = 4.167 \text{ kHz.}$$

- d. Another frequency is measured with the first TCNT = \$100 and the second TCNT=\$010. What is the frequency of the square wave?

$$\text{Number of counts} = \text{\$400} - \text{\$100} + \text{\$010} = \text{\$310} = 784$$

$$784 \text{ counts} \times 10^{-6} \text{ sec/count} = 7.84 \times 10^{-4} \text{ sec/period} \rightarrow 1.275 \text{ kHz}$$

---

<sup>1</sup> The FC in 68FC12 refers to a new semiconductor technology developed by a Colonel Saunders from Kentucky.

- e.
4. Give short answers to the following questions: (10 points)

a. Why must a latch be used to interface an output device to the data bus?

**Because the data bus is active at all times and so a latch and a timed latch clock is needed to capture the correct output data.**

b. Why must a tri-state gate be used to interface an input device to the data bus?

**To allow multiple sources to be used in the system.**

c. In the HC12, why does the CPU automatically push all registers on the stack before transferring control to the user's ISR?

**To preserve the machine context for returning to the interrupted program.**

d. In the HC12, why does the CPU automatically set the I bit in the condition code register before transferring control to the user's ISR?

**To mask further interrupts during processing of the ISR.**

e. What is interrupt latency?

**The amount of time between the interrupt request generated by the hardware and the start of the execution of the interrupt service routine.**