EE371 Third Semester Test - Thursday December 2, 2004
35 points, 16.67% of Final Grade

Please put your name on the outside of the paper also. Name _____KEY_____

Notation: An active-low signal is denoted by an '*", i.e. ADR_OK* is a signal asserted low.

1. Why must a tri-state gate be used to interface an input device to the data bus? (2 points)
The tri-state gate allows multiple sources to source their data, one at a time, on to the data bus. The CPU's read control signal must control the tri-state gate's enable.

2. Why must a latch be used to interface an output device to the data bus? (2 points)
The data bus is active all the time with input data from input devices, and data flowing to and from memory. To be able to output specific data to an output device at a specific time, a latch must be used which is clocked by the write control signal.

3. Design the hardware for a tristate enable signal in an input interface that uses the 74LS138 decoder shown below to decode the 6-bit address ADR[5:0] = $27. The ADR_OK*output from the decoder is to be anded with an IO_RD* signal to generate an active low tristate enable EN*. (5 points)

One solution would be to make the following connections:

E1* = ADR3
E2* = ADR4
E3 = ADR5
A2 = ADR2
A1 = ADR1
A0 = ADR0

AND O7* and IO_RD* to produce EN* using an active-low input, active-low output AND gate (and OR gate).

4. In the HC12, Port T is a bidirectional port. Write a short segment of code that illustrates how to initialize Port T so that bits 7, 4 and 3 may be used as outputs and 6, 5, 2, 1 and 0 may be used as inputs. (3 points)

```
DDRT    EQU     $AF
        bset    DDRT,%10011000  ; Make bits 7, 4,. and 3 outputs
        bclr    DDRT,%01100111  ; Make bits 6, 5, 2, 1, and 0 inputs (default state)
```

5. The TCNT register is receiving an 8 MHz clock.
   a. How many clock cycles will constitute a delay of 5.8 milliseconds? (2 points)
   5.8 ms * $8x10^6$ clocks/sec = 46,400

   b. If you are using an output compare with interrupts to delay 5.8 milliseconds, can this be done without multiple interrupts? (2 points)
   Yes, the required delay is less than 8.192 ms assuming an 8 MHz clock.

6. Give short answers to the following:
   a. What are polled interrupts? (3 points)

An interrupt system in which all interrupting devices share a single interrupt request line. When an interrupt occurs, the program must interrogate, or poll, each of the devices in turn to determine which has generated the interrupt.

   b. The HC12 is a vectored interrupt processor. Described how the HC12 (operating without the D-bug12 monitor) uses a vector to find the correct interrupt service routine after an interrupt occurs. (3 points)

The address of the specific ISR stored in a specific memory location called the vector location. When an interrupt is caused by that device, the HC12 masks further interrupts, pushes all registers on the stack, check for highest priority interrupt and retrieves the address from the vector location.

   c. What advantage does a vectored interrupt system have over a polled interrupt system? (2 points)

The time taken to start the interrupt service routine is shorter in a vectored system.

7. Interrupt latency is the time interval between an interrupt request and the start of the interrupt service routine.
   a. Give two components of interrupt latency. (2 points)

Time to complete the current instruction
Time to push the registers on the stack
Time to fetch the ISR address,

   b. Describe how you could measure interrupt latency in the lab using the lab board and other lab instrumentation (hint: such as the oscilloscope and a function generator). (3 points)

You could take a square-wave signal from the function generator to drive one of the external interrupt lines, such as IRQ. The interrupt service routine would then set an I/O bit and then reset it. The time between the falling edge of the IRQ signal and the rising edge of the output bit, minus the known number of clock cycles needed to set the bit will be a measure of the latency.

8. Give short answers to the following for an A/D system:
   a. Define conversion time. (2 points)

Time from the start of the conversion to when the A/D has completed the conversion. The conversion time must be less than ½ the maximum frequency in the signal to avoid aliasing.

   b. What is a sample-and-hold? (2 points)

A device, usually a capacitor and an electronic switch, with a very short aperture time that samples, and then holds constant, the analog signal for the A/D.

   c. How do you calculate the required aperture time for a sample-and-hold. (2 points)

$$t_{AP} = \frac{1}{2pf_{MAX}2^n}$$