

EE 371 Last Semester Test -
Thursday December 11, 2003
3 pages, 10 questions, 45 points, 15% of Final Grade

Please put your name on the outside of the paper also Name _____ KEY _____

1. Two computers are to be connected using their COM ports: (8 points)
 - a. For this to work, what operational parameters need to be specified?
bit rate, coding scheme, #stop bits, parity, #data bits, handshaking or data flow
 - b. In this application, what is meant by “data flow” synchronization?
Being able to synchronize transfer of data at a higher level than the bit level, e.g. a faster computer sending data to a slower one; this allows the slower computer to stop the faster computer.
 - c. What are two ways data flow synchronization can be achieved?
Hardware handshaking (RTS, CTS) and software (XON, XOFF)
2. How does an asynchronous serial port achieve synchronization of the bits it is sending or receiving? (2 points)
By starting each character with a start bit.
3. A system is to be designed to transfer serial data from one place to another over a distance of 200 feet. Data is to be transferred in one direction only, there is no data flow problem. Data transfer rate is to be a minimum of 100 kilobits/second. You are to compare an asynchronous serial port approach (SCI) with a synchronous serial port (SPI) approach. (4 points)
 - a. How many wires will be needed to connect the two systems (including the ground wire)?
SCI: 2 SPI: 3
 - b. For this distance and data rate, what signaling interface standard would you propose?
Anything but TTL and RS232.
4. An 8-bit successive approximation A/D converter has a 1 megahertz clock. What is the maximum frequency it can convert without aliasing? (3 points)
 **$1 \text{ sample}/8 \text{ clocks} * 10^6 \text{ clocks/sec} = 125 \text{ kilo samples/sec}$
 $f_{\text{sample}} = 2 * f_{\text{max}}$, therefore $f_{\text{max}} = 62.5 \text{ kHz}$.**
5. An analog input signal ranges from 0 to +5 volts with 10 mV of noise. How many bits of resolution is the best you can achieve when converting this to a digital value? (3 points)
 $5\text{v}/10 \text{ mV} = 500$ requires 9 bits (the answer I was looking for but the way the question reads I accept 8 bits.)

6. In the HC12 world, what is the difference between an interrupt mask bit and an interrupt enable bit? (6 points)
The interrupt mask acts globally on all interrupting sources; a 1 mask (stops) interrupts and 0 unmask (allows) interrupts.
An interrupt enable bit acts locally on an individual interrupting source; a 1 enables the interrupt and 0 disables.

7. The HC12 timer channel 3 interrupt flag (C3F) is bit 3 in the TFLG1 Timer Interrupt Flag 1 register (\$008E). Show a snippet of code that you would use to reset this flag. (2 points)

```
C3F    EQU    %00001000
TFLG1  EQU    $8E
```

```
ldaa  #C3F
staa  TFLG1
```

8. The infamous 68HC12 processor has a 12-bit timer subsystem similar to the HC12's. It has a 12-bit TCNT register with one 12-bit output compare register and similar flags and controls. Assume that it has a 1 megahertz clock. (6 points)

- a. What is the interval between timer overflows?

$$2^{12} = 4096 * 10^{-6} = 4.096 \text{ ms}$$

- b. Assuming the present value of the TCNT register is \$D18 what value should be loaded into the output compare register to create a delay of

- i) 100 microseconds? _____

$$100 \text{ microseconds} = 100 \text{ counts} = \$64 \text{ counts}; \$D18 + \$64 = \$D7C$$

- ii) 1 millisecond? _____

$$1 \text{ ms} = 1000 \text{ counts} = \$3E8 \text{ counts}; \$D18 + \$3E8 = \$100 \text{ (modulo 4096 addition)}$$

9. When writing a program that uses an interrupt, there is a recommended way to organize your program (a template). List the steps in this template as pseudo-code to be used in such a program. Assume that the code is to be run on an EVB with the Dbug-12 monitor. (5 points)

```

;*****
; 1: Initialize all hardware
; Any hardware initialization, e.g. timer,
; should be done here
;*****
; 2: Initialize the interrupt vector in D-Bug12
;*****
; 3: Clear any flags that could cause interrupts
;*****
; 4: Enable the interrupting subsystem
; Now it is safe to enable the interrupts
;*****
; 5: Unmaks HC12 interrupts
; Unmask I-bit
    cli
;*****
; 6: Go into the foreground job
foreground:
;    ...
;    ...
    bra    foreground
;*****
;*****
; 7: Here is the background job or
; Interrupt Service routine (ISR)
ISR:
;*****
; 8: Re-enable and unmask higher priority
; interrupts as needed
;*****
; 9: Do the background or interrupt specific task
;*****
; 10: Reset any interrupting flags
;*****
; 11: Return from the ISR
    rti        ; Return to interrupted prog

```

10. External memory chips are to add a total of 8K bytes of RAM in address \$4000 to \$5FFF to a CPU which has an 8-bit data, 16-bit address and RD* and WR* control signals. The stock room has an abundance of 4K x 8 bit chips plus a variety of SSI gates, 3-8 decoders, 4-16 decoders, latches and tri-state gates. Complete the diagram below showing how the memory is to be interfaced to the CPU. (6 points)

