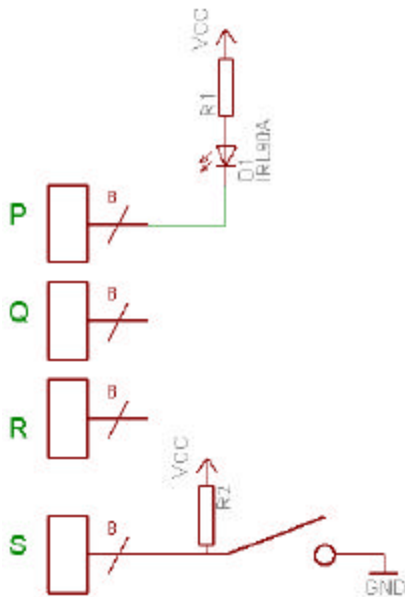


Please put your name on the outside of the paper also.  
Hand in the test folded so your name shows on the outside.

Name \_\_\_key\_\_\_\_\_

1. A mythical microprocessor, the 12FC68, has two, 8-bit output ports (P and Q) and two, 8-bit input ports (R and S). Assume that a set of 8 switches is connected to Port S and a set of 8 LEDs is connected to Port P as shown below. Describe (a diagram would be nice) how you would implement a scheme using these resources (plus any others you would like, i.e. more switches, buffers, latches, etc.) that would allow you to input data from the switches only after the user has completed entering new data, and then to display the 8-bit data on the LEDs. Note that if you add hardware you must show how it is done. Remember that the boss over there at Two Dot Engineering is a stingy old cuss who wants the hardware to be as simple and cheap as possible. (10 points)



Add one push button switch, properly connected with a pull up resistor, to one of the bits, say bit-7 on Port R. The switch would not have to be debounced in hardware if it is debounced in software. The switch is to be used by the user to indicate that the data has been entered into the 8 switches on PORTS.

2. Now, assuming the hardware you have proposed in the previous question, describe, from a high-level, using pseudo-code, how you would:

- a. Input data from the switches (5 points)

```

SPIN WHILE PORTR-7 is high
Get data from PORTS
Debounce PORTR-7
SPIN WHILE PORTR-7 is low
    
```

- b. Output data to the LEDs. (5 points)

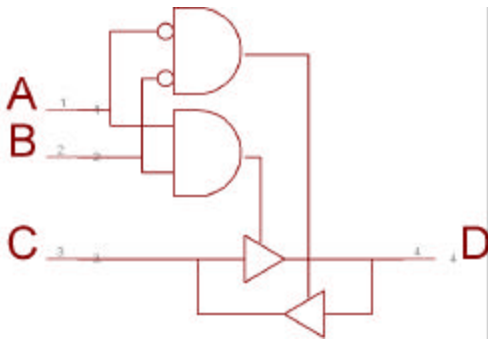
```

Complement the data to display correctly
Store the data to PORTP
    
```

3. In a general computer system with external address, data and control busses, how are multiple input devices distinguished from one another? (Your answer must consider both hardware and software concerns.) (5 points)

Each input device is connected to a data bus through a tri-state gate whose enable is controlled by an address decoder and a control signal from the CPU. Thus each input device has its unique address. The software must provide either an input instruction with a port address in a separate I/O addressing scheme or memory reference instructions with an address in a memory mapped scheme.

4. The chip shown below is a 74LSxxx. Fill in the truth table describing its operation. (3 points)



A	B	Function
0	0	C tri-state, D transfers to C
0	1	Both C and D tri-state
1	0	Both C and D tri-state
1	1	D tri-state, C transfers to D

5. What features does the HC12 have to allow you to manage multiple sources of interrupts? (5 points)

Global control with the I bit and CLI and SEI instructions.

Individual control with enable bits for each interrupting source.

Vectored interrupts with a vector for each interrupting source.

A programable hardware priority scheme for dealing with simultaneous interrupts.

6. Describe how the HC12 manages to transfer control to the correct interrupt service routine for any particular interrupt in an embedded system without a Dbug-12 monitor. (4 points)

A specific interrupt vector location is programmed with the address of the interrupt service routine (vectored interrupts) or the polling method can be used for multiple sources on the IRQ line.

7. List three of the four methods of synchronizing I/O software. (3 points)

S/W delay loops, handshaking/polling, interrupts