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CHAPTER 7

M68HC12 PARALLEL I/O

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OBJECTIVES

This chapter describes the parallel I/O capabilities of the M68HC12. You will find that almost all I/O features must be programmed or initialized before use by setting and resetting bits in control registers. Examples show how this is done.

- 7.1 Introduction
- 7.2 MC68HC812A4 and MC68HC912B32
- 7.3 Operating Modes
 - Normal Single-chip Mode
 - Normal Expanded Mode
 - Mode Register
- 7.4 The Programmer's I/O Model
- 7.5 M68HC12 Parallel I/O Ports
 - Ports A and B
 - Port
 - Port D
 - Port E
 - Port F
 - Port G
 - Port H and Port J
 - Port S
 - Port T
 - Port AD
- 7.6 Data Direction Registers
- 7.7 Input and Output Pin Electronics
 - Pull-up Control
 - Reduced Drive
- 7.8 I/O Software
 - Real-time Synchronization
 - Polled I/O
- 7.9 Hardware Handshaking I/O
- 7.10 Chapter Summary Points

This chapter has covered the parallel I/O capabilities of the M68HC12 microcontroller. The summary points are:

- ! The MC68HC812A4 and MC68HC912B32 versions have differing I/O capabilities.
- ! When ports are not being used for expanded mode or other I/O they may be used for general purpose parallel I/O.
- ! Ports A, B, C, and sometimes D may not be used for I/O when in expanded modes.
- ! All I/O ports have programmable functions.
- ! Bidirectional ports have Data Direction Registers to specify the data flow direction.
- ! Port S shares functions with parallel I/O and the serial I/O.
- ! Port AD shares functions with parallel I/O and the A/D converter system.